What is claimed is:

1. A contact process for a semiconductor device containing a base region of a first conductivity type formed on a semiconductor substrate, said contact process comprising the steps of:

heavily doping a first surface of said base region for forming a first shallow layer of said first conductivity type on said base region;

depositing an insulator on said first shallow layer;

etching said insulator and first shallow layer for forming a contact hole thereof to thereby expose a sidewall of said first shallow layer and a second surface of said base region;

thermally driving said first shallow layer more deeply into said base region;

heavily doping said second surface of said base region through said contact hole for forming a second shallow layer of a second conductivity type opposite to said first conductivity type on said second surface of said base region; and

filling a metal in said contact hole for contacting said sidewall of said first shallow layer and said second shallow layer.

2. The contact process of claim 1, wherein said first shallow layer is formed by an ion implantation.

3. The contact process of claim 2, wherein said ion implantation comprises an inclined ion implantation.

4. The contact process of claim 3, wherein said inclined ion implantation is performed with an inclined angle of about 45 degrees.

5. The contact process of claim 1, wherein said insulator is etched by a wet etching.

6. The contact process of claim 1, wherein said first shallow layer is etched by a plasma etching.

7. The contact process of claim 6, wherein said plasma etching comprises a vertical over-etching of a thickness of said base region.

8. The contact process of claim 1, further comprising forming a pad oxide on said sidewall of said first shallow layer prior to said thermally driving said first shallow layer so as to prevent said first shallow layer from outdiffusion through said sidewall thereof during said thermally driving said first shallow

layer.

9. The contact process of claim 8, wherein said pad oxide is formed by a low-temperature oxide growth.

10. The contact process of claim 1, further comprising an annealing after depositing said insulator.

11. The contact process of claim 1, further comprising an annealing after forming said second shallow layer.

12. The contact process of claim 1, further comprising a blanket etching to said second shallow layer prior to said filling a metal in said contact hole.

13. A contact structure for a semiconductor device containing a base region of a first conductivity type formed on a semiconductor substrate, said contact structure comprising:

a first shallow layer of a first conductivity type formed on a first surface of said base region;

an insulator covered on said first shallow layer;

a contact hole extending through said insulator and first shallow layer to thereby expose a sidewall of said first shallow layer and a second surface of said base region;

a second shallow layer of a second conductivity type opposite to said first conductivity type formed on said second surface of said base region; and

a metal filled in said contact hole for contacting said sidewall of said first shallow layer and said second shallow layer.

14. The contact structure of claim 13, wherein said first shallow layer is deeper than said second shallow layer into said base region.

15. The contact structure of claim 13, wherein said first and second shallow layers are not overlapped with each other.